

## Claims

We claim:

1           1. A scan test circuit design imbedded within an integrated circuit chip having  
2 a test clock signal, comprising:  
3                 at least one scan-in terminal coupled to receive a test stimulus input  
4 data;  
5                 at least one scan-out terminal to output testing resultant data;  
6                 at least one scan chain group each having a clock domain, the at least  
7 one scan chain group coupled between one of the at least one scan-in terminal and  
8 one of the at least one scan-out terminal, wherein the test clock signal enables the  
9 testing of each of the at least one scan chain group, each scan chain group has a  
10 corresponding test mode signal to shift the test stimulus input data at a shift clock  
11 rate derived from the corresponding clock domain, wherein each at least one scan  
12 chain group comprises,  
13                 a demultiplexer unit, having an input, an enable input, a first output and  
14 a second output, the input coupled to receive the test stimulus input data, the  
15 enable input coupled to receive the test clock signal, the first output coupled  
16 to a functional input for the portion of the integrated circuit chip being tested,  
17                 a first multiplexer unit, having a first input, a second input, an enable  
18 input, and an output, the first input coupled to the second output of the  
19 demultiplexer unit, the enable input coupled to receive a simultaneous test  
20 mode signal,  
21                 a scan chain, having an input, a control input, and an output, the input  
22 coupled to the output of the first multiplexer unit, the scan chain having a  
23 corresponding scan chain clock domain at a predetermined frequency, and  
24                 a second multiplexer unit, having a first input, a second input, an  
25 enable input, and an output, the first input coupled to the output of the scan  
26 chain, the second input coupled to receive functional output data from the

27 portion of the integrated circuit chip being tested to supply testing resultant  
28 data at the output;

29 a controlling demultiplexer coupled to the second output of one  
30 demultiplexer unit and coupled to receive the simultaneous test mode signal and a  
31 plurality of test mode signals for each scan chain group to generate control signals  
32 to be coupled to the second input of each first multiplexer unit to control the  
33 concurrent shifting of the test stimulus input data into each scan chain at the  
34 predetermined frequency;

35 a clock control mechanism coupled to receive the test clock signal, a  
36 test mode select pin inputs, a scan enable signal, functional clock and enable  
37 signals corresponding to each of the at least one scan chain groups to generate a  
38 control signal for each scan chain, the plurality of test mode signals for each scan  
39 chain group and the simultaneous test mode signal,

40 wherein the clock control mechanism coupled to the control input of  
41 each scan chain of the at least one scan chain group to enable one scan chain to  
42 shift test stimulus input data when the scan enable signal is enabled and the test  
43 clock signal is enabled, the clock control mechanism coupled to each scan chain to  
44 enable simultaneous capture of each of the at least one scan chain group when the  
45 scan enable, the test clock, and the simultaneous test mode signals are enabled;  
46 and

47 a controlling multiplexer coupled to the output of each scan chain and  
48 coupled to receive each test mode signal to generate a control signal for the second  
49 multiplexer of the least significant of the at least one scan chain group.

1 2. An integrated circuit chip as recited in claim 1, wherein the clock control  
2 mechanism comprises:

3 a scan logic device coupled to receive a test clock and a scan enable  
4 signal to generate an enable signal that detects the rising edge on the scan enable  
5 signal and an enable signal that detects a rising or falling transition on the scan  
6 enable signal;

7                   at least one clock generator for a respective one of the at least one  
8 scan chain groups coupled to receive both enable signals generated by the scan  
9 logic device, the test clock signal, the function enable and clocking signals  
10 corresponding to the at least one scan chain group to produce a clock signal for  
11 controlling the scan chain of the respective at least one scan chain group; and  
12                   a decode logic unit, having the test mode select pins, the decode logic  
13 unit coupled to each one of the at least one clock generators to provide a test mode  
14 delta signal, a VLCT mode signal, the test mode signals corresponding to each  
15 respective one of the at least one scan chain groups, and the simultaneous test  
16 mode signal for simultaneous testing of all scan chain groups.

1     3. An integrated circuit chip as recited in claim 2, wherein the scan logic device  
2 comprises:

3                   a DQ flip-flop, having a clock input, a D-input and a Q-output, the clock input  
4 coupled to receive the test clock signal, the D-input coupled to receive the scan  
5 enable signal;

6                   an inverter coupled to the Q-output;

7                   an AND gate, having a first input, a second input, and an output, to generate  
8 at the output the enable signal that detects the rising edge on the scan enable  
9 signal, the first input coupled to receive the scan enable signal, the second input  
10 coupled to the inverter; and

11                  a NOR gate, having a first input, a second input and an output, to generate at  
12 the output the enable signal that detects a rising or falling transition on the scan  
13 enable signal, the first input coupled to the Q-output, the second input coupled to  
14 receive the scan enable signal.

1     4. An integrated circuit chip as recited in claim 2, wherein the clock generator  
2 comprises:

3                   a first inverter coupled to receive the VLCT mode signal;

4                   a second inverter coupled to receive the enable signal that detects the  
5 rising edge on the scan enable signal;

6 a first AND gate coupled to the first inverter and the second inverter;  
7 a first OR gate coupled to receive the enable signal that detects a  
8 rising or falling transition on the scan enable signal and the test mode delta signal;  
9 a third inverter coupled to the first OR gate;  
10 a second AND gate coupled to the third inverter and coupled to receive  
11 one of the test mode signals corresponding to each respective one of the at least  
12 one scan chain groups;  
13 a second OR gate coupled to the first and second AND gates;  
14 a first DQ flip-flop, having a D-input, an enable input and a Q-output,  
15 the D-input coupled to the second OR gate;  
16 a fourth inverter, having an input and an output, the input coupled to  
17 receive the test clock signal, the output coupled to enable input of the first DQ flip-  
18 flop;  
19 a third AND gate coupled to the Q-output of the first DQ flip-flop and  
20 coupled to receive the test clock signal;  
21 a NOR gate coupled to the third AND gate and coupled to receive a  
22 polarity test clock signal;  
23 a second DQ flip-flop, having a D-input, an enable input and a Q-  
24 output, the D-input coupled to the NOR gate;  
25 a fourth inverter, having an input and an output, the input coupled to  
26 receive the functional clock signal corresponding to the at least one scan chain  
27 group, the output coupled to enable input of the second DQ flip-flop;  
28 a fourth AND gate coupled to the Q-output of the second DQ flip-flop  
29 and coupled to receive the functional clock signal corresponding to the at least one  
30 scan chain group; and  
31 a multiplexer unit, having a first input, a second input, a control input  
32 and an output, to provide the clock signal for controlling the scan chain of the  
33 respective at least one scan chain group, the first input coupled to the fourth AND  
34 gate, the second input coupled to receive the functional enable signal corresponding  
35 to the at least one scan chain group, the control input coupled to a test mode signal.

1 5. An integrated circuit chip as recited in claim 2, wherein the decode logic unit  
2 comprises:

3 a plurality of DQ flip-flops, each having a D-input, a Q-output, an  
4 inverted Q-output, and a clock input, each clock input coupled to receive the test  
5 clock signal, each D-input coupled to a respective test mode select pin;

6 a plurality of NOR gates, each having a first input, a second input and  
7 an output, each first input coupled to a respective test mode select pin, each second  
8 input coupled to a respective Q-output of the plurality of DQ flip-flops; and

9 a OR gate coupled to the output of each of the plurality of NOR gates  
10 to generate the test mode delta signal

11 a plurality of multi-input AND gates, each having a number of inputs  
12 corresponding to the number of DQ flip-flops and an output, each input coupled to a  
13 Q-output or an inverted Q-output in a specified pattern to generate intermediate  
14 signals for each test mode corresponding to the at least one scan chain group and to  
15 generate the simultaneous test mode signal for simultaneous testing of all scan  
16 chain groups;

17 a first inverter coupled to receive the first intermediate signal for a  
18 respective test mode corresponding to the at least one scan chain group;

19 a second inverter coupled to receive the second intermediate signal for  
20 a respective test mode corresponding to the at least one scan chain group;

21 a third inverter coupled to receive the third intermediate signal for a  
22 respective test mode corresponding to the at least one scan chain group

23 a first AND gate coupled to the first and second inverter to provide the  
24 test mode signal corresponding to the third scan chain group;

25 a second AND gate coupled to the first and third inverter to provide the  
26 test mode signal corresponding to the second scan chain group;

27 a third AND gate coupled to the second and third inverter to provide  
28 the test mode signal corresponding to the second scan chain group;

29 a OR gate coupled to the first, second and third AND gates to generate  
30 the VLCT mode signal.

1           6. A method for testing an integrated circuit chip having at least two clock  
2 domains at respective domain test clock rates corresponding to at least two scan  
3 chain groups, using a very low cost test (VLCT) platform -Automatic Test Pattern  
4 Generator (ATPG), comprising:

5           (a) clocking a test stimulus input data into each scan chain of each  
6 said clock domain sequentially by clocking the test stimulus input data into one scan  
7 chain and disabling the clocks of the other respective scan chain groups to hold  
8 these other respective scan chain groups static, clocking said test stimulus input  
9 data at a shift clock rate derived from at least one of said scan chain clock domains;

10           (b) capturing on all scan chain groups resultant data simultaneously at  
11 a predetermined frequency corresponding to one of the plurality of scan chain  
12 groups domain test clock rate;

13           (c) storing resultant data from one of the plurality of scan chain groups  
14 that corresponds with the predetermined frequency;

15           (d) repeating steps (a) – (c) at a corresponding frequency for each of  
16 the at least two scan chain groups.

1           7. A method for stuck-at fault testing an integrated circuit chip having at least  
2 two clock domains at respective domain test clock rates corresponding to at least  
3 two scan chain groups, using a very low cost test (VLCT) platform for a full device  
4 scan Automatic Test Pattern Generator (ATPG), comprising:

5           (a) applying test mode select code signal to a plurality of test mode  
6 select pins of a clock control mechanism for controlling the shift scan inputs of the at  
7 least two scan chain groups;

8           (b) shifting a test stimulus input data into each scan chain of each said  
9 clock domain sequentially by shifting the test stimulus input data into one scan chain  
10 and disabling the clocks of the other respective scan chain groups to hold these  
11 other respective scan chain groups static, shifting said test stimulus input data at a  
12 shift clock rate derived from at least one of said scan chain clock domains;

13           (c) capturing on all scan chain groups resultant data simultaneously at  
14 a predetermined frequency corresponding to one of the plurality of scan chain

groups domain test clock rate by applying two capture pulses separated by the twice the period of the corresponding domain test clock rate;

(d) storing resultant data from one of the plurality of scan chain groups that corresponds with the predetermined frequency;

(e) repeating steps (a) – (d) at a corresponding frequency for each of the at least two scan chain groups.

8. A method for at-speed transition fault testing an integrated circuit chip having at least two clock domains at respective domain test clock rates corresponding to at least two scan chain groups, using a very low cost test (VLCT) platform for a full device scan Automatic Test Pattern Generator (ATPG), comprising:

(a) applying test mode select code signal to a plurality of test mode select pins of a clock control mechanism for controlling the shift scan inputs of the at least two scan chain groups;

(b) clocking a test stimulus input data into each scan chain of each said clock domain sequentially by clocking the test stimulus input data into one scan chain and disabling the clocks of the other respective scan chain groups to hold these other respective scan chain groups static, clocking said test stimulus input data at a shift clock rate derived from at least one of said scan chain clock domains;

(c) capturing on all scan chain groups resultant data simultaneously at a predetermined frequency corresponding to one of the plurality of scan chain groups domain test clock rate by applying two capture pulses separated by the twice the period of the corresponding domain test clock rate;

(d) storing resultant data from one of the plurality of scan chain groups that corresponds with the predetermined frequency;

(e) repeating steps (a) – (d) at a corresponding frequency for each of the at least two scan chain groups.